AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented) A system comprising,

a configurable mask;

an AND gate; and

a cache having one or more configurable bits that are configurable to identify one or more sets having at least one line of information storage and a tag to identify a line of information storage, wherein the configurable bits are ANDed to the configurable mask.

2. (Previously Presented) The system of claim 1, wherein the number of sets is equal to the binary value of the configurable mask plus one.

3. (Cancelled)

4. (Cancelled)

5. (Previously Presented) The system of claim 1, wherein the configurable bits are set index bits when configured to identify the set having at least one line of information storage and the configurable bits are tag bits when configured to identify the line of information storage.

6. (Previously Presented) The system of claim 5, wherein the cache includes a plurality of lines of information storage and each line of information storage includes at least one set index bit.

7. (Previously Presented) The system of claim 6 wherein the lines of data storage include no tag bits.

8. (Previously Presented) The system of claim 5, wherein the cache includes a plurality of lines of information storage and each line of information storage includes at least one tag bit.

9. (Previously Presented) The system of claim 8, wherein the lines of data storage include no set index bits.

10. (Previously Presented) The system of claim 5, wherein the configurable bits are configured as tag bits and reconfigured as set index bits.

11. (Previously Presented) The system of claim 10, wherein all entries in the cache are invalidated prior to reconfiguring the configurable bits so that no address holds valid data prior to the configurable bits being reconfigured as set index bits.

12. (Previously Presented) The system of claim 5, wherein the configurable bits are configured as set index bits and reconfigured as tag bits.

13. (Previously Presented) The system of claim 12, wherein all entries in the cache are invalidated prior to reconfiguring the configurable bits so that no address holds valid data prior to the configurable bits being reconfigured as tag bits.

14. (Cancelled)

15. (Previously Presented) A method of configuring cache formed on an integrated circuit comprising,

associating one or more bits as configurable bits that are configurable to identify one or more sets having at least one line of information storage and a tag to identify a line of information storage; and

ANDing the configurable bits to a configurable mask.

16. (Previously Presented) The method of claim 15, wherein the number of sets is equal to the binary value of the configurable mask plus one.

17. (Previously Presented) The method of claim 15, wherein the configurable bits are configurable through software.

18. (Previously Presented) The method of claim 15, wherein the cache includes a plurality of cache lines.

19. (Previously Presented) The method of claim 15, wherein the configurable bit is reconfigurable from a tag bit to a set index bit.

20. (Previously Presented) The cache of claim 15, wherein the bits are reconfigurable from set index bits to tag bits.

21. (Previously Presented) A node, comprising:

an AND gate;

a configurable mask;

a processor; and

cache formed on an integrated circuit coupled to the processor to store information for retrieval by the processor, the cache having one or more configurable bits that are configurable as one or more set index bits and one or more tag bits, wherein the configurable bits are ANDed to the configurable mask.

22. (Previously Presented) The node of claim 21, wherein the cache includes a plurality of lines of information storage, further comprising one or more configurable bits that are configurable as tag bits and set index bits in each line of the cache.

23. (Previously Presented) The node of claim 21, wherein the configurable bits are reconfigurable from tag bits to set index bits.

24. (Previously Presented) The node of claim 21, wherein the configurable bits are reconfigurable from set index bits to tag bits.

25. (Previously Presented) A method of configuring cache formed on a integrated circuit and having a plurality of address bits, comprising

setting at least one of the cache address bits as one of a tag bit and a set index bit; and

ANDing the configurable bits to a configurable mask,

wherein the cache includes a plurality of lines and each line includes the plurality of address bits.

26. (Cancelled)

27. (Original) The method of claim 25, wherein the cache includes a plurality of information storage locations identified by the address bits, further comprising:

setting at least one of the cache address bits as a tag bit;

placing information in at least one of the information storage locations;

invalidating information in all information storage locations in the cache; and

reconfiguring the bit from a tag bit to a set index bit.

28. (Original) The method of claim 25, wherein the cache includes a plurality of information storage locations identified by the address bits, further comprising:

setting at least one of the cache address bits as a set index bit;

placing information in at least one of the information storage locations;

invalidating information in all information storage locations in the cache; and

reconfiguring the bit from a set index bit to a tag bit.

29. (Previously Presented) An article of manufacture comprising:

a computer readable medium having stored thereon instructions which, when executed by a processor, cause the processor to

associate one or more bits as configurable bits that are configurable to identify one or more sets having at least one line of information storage and a tag to identify a line of information storage; and

AND the configurable bits to a configurable mask, wherein the number of sets is equal to the binary value of the configurable mask plus one.

30. (Original) The article of manufacture of claim 29, wherein the cache includes a plurality of lines and each line includes a plurality of address bits, further comprising setting at least one of the cache address bits in each line of cache as one of a tag bit and a set index bit.